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FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Attorney Docket No.: 12172-004530US	Application No.: 09/057,861
	Applicant: Howard G. Sachs	
	Filing Date: April 9, 1998	Group: ~~2784~~ ~~2758~~ 2154

Reference Designation — **U.S. PATENT DOCUMENTS** — Page 1

Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-class	Translation (Yes/No)

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

VV. AA	Gray et al., "Static Instruction Scheduling for the HARP Multiple-Instruction-Issue Architecture", Technical Report 142, University of Hertfordshire, Hatfield, Herts UK, October 1992
VV. AB	Stevens, "An Introduction to the Hatfield Superscalar Scheduler", Technical Report No. 316, University of Herfordshire, Hatfield, Herts UK, Spring 1998
VV. AC	Stevens et al., "iHARP: A Multiple Instruction Issue Processor", Technical Report No. 125, Hatfield Polytechnic, November 1991

EXAMINER V. Vu — DATE CONSIDERED 12-3-99

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VV.	AA	Adams et al., "HARP: A Statically Scheduled Multiple-Instruction-Issue Architecture and its Compiler", Technical Report 163, University of Hertfordshire, Hatfield, Herts UK, pp. 1-8, September 1993
	AB	Arya et al., "An Architecture for High Instruction Level Parallelism", pp. 1-21, 1/1995.
	AC	Beck et al., "The Cydra 5 Minisupercomputer: Architecture and Implementation", J. Supercomputing, 7:143-179 (1993)
	AD	Butler, et al., "Single Instruction Stream Parallelism Is Greater than Two", 1991 ACM, pp. 276-286
	AE	Chang et al., "Comparing Static and Dynamic Code Scheduling for Multiple-Instruction-Issue Processors", Proceedings of the 24th International Symposium on Microarchitectures - MICRO24, pp. 1-9, 1991
	AF	Chen, "The Effect of Code Expanding Optimizations on Instruction Cache Design", IEEE Transactions on Computers, 42(9) pp. 1045-1057, September 1993
	AG	Colwell, et al., "A VLIW Architecture for a Trace Scheduling Compiler", IEEE Transactions on Computers, 37(8) pp. 967-979, August 1988
	AH	Conte, "Trade-Offs in Processor/Memory Interfaces for Superscalar Processors", MICRO-25, The 25th Annual International Symposium on Microarchitecture, December 1992
	AI	Dehnert et al., "Compiling for the Cydra 5", J. Supercomputing, 7, pp. 181-227, May 1993
	AJ	Fisher et al., "Instruction-Level Parallel Processing", Science, 253, pp. 1233-1241, September 1991
	AK	Fisher et al., "Parallel Processing: A Smart Compiler and a Dumb Machine", ACM-Sigplan 84 Compiler Construction Conference, 19(6), June 1984
	AL	Fisher, "Trace Scheduling: A Technique for Global Microcode Compaction", IEEE Transactions on Computers, C-30(7):478-490 July 1981
	AM	Fisher, "Very Long Instruction Word Architectures and the ELI-512", Proceedings of the 10th Symposium on Computer Architecture, ACM Press, pp.140-150 (1983)
	AN	Gee et al., "Cache Performance of the SPEC92 Benchmark Suite", IEEE MICRO, pp. 17-27, August 1993
	AO	Gwennap, "Visionaries See Beyond Superscalar", Microprocessor Report, pp. 18-19, December 6, 1993
	AP	Hennessy et al., "Computer Technology and Architecture: An Evolving Interaction", IEEE Computer, pp.18-29, September 1991
	AQ	Hsu et al., "Highly Concurrent Scalar Processing", 13th International Symposium on Computer Architecture, pp. Tokyo, 1986, pp. 1-10
	AR	Johnson, "Superscalar Microprocessor Design", Prentice-Hall, Englewood Cliffs, New Jersey, 1991
	AS	Karl, "Some Design Aspects for VLIW Architectures Exploiting Fine-Grained Parallelism", Proceedings of the 5th International PARLE Conference, pp. 582-599, June 1993
	AT	Lam et al., "Limits of Control Flow on Parallelism", Computer Architecture News, 20(2):46-57 (1992)
	AU	Lam, "Software Pipelining: An Effective Scheduling Technique for VLIW Machines", Proceedings of ACM SIGPLAN '88 Conference on Programming Language Design and Implementation, pp. 318-328, June 1988
	AV	Mahlke et al., "Effective Compiler Support for Predicated Execution Using the Hyperblock", MICRO 25, Proceedings of the 25th Annual International Symposium on Microarchitectures, IEEE Computer Society Press, pp. 45-54, December 1992
	AW	Mahlke et al., "Sentinel Scheduling for VLIW and Superscalar Processors", In Proceedings of ASPLOS V,27(9) pp. 238-247, September 1992

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VV.	AX	Moon et al., "An Efficient Resource-Constrained Global Scheduling Technique for Superscalar and VLIW Processors", MICRO 25, Proceedings of the 25th Annual International Symposium on Microarchitecture, pp. 55-71, December 1992
	AY	Nicolau et al., "Measuring the Parallelism Available for Very Long Instruction Word Architectures", IEEE Transactions on Computers, C-33(11), pp. 968-976, November 1984
	AZ	Oyang et al., "A Cost Effective Approach to Implement A Long Instruction Word Microprocessor", Computer Architecture News, 18(1), March 1990, pp. 59-72
	BA	Pan et al., "Improving the Accuracy of Dynamic Branch Prediction Using Branch Correlation", Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-V), Vol. 27, pp. 76-84 (1992)
	BB	Park et al., "On Predicated Execution", Technical Report HPL-91-58, Hewlett-Packard Laboratories May 1991
	BC	Rau, "Cydra™ 5 Directed Dataflow Architecture", Proceedings of COMPCON 1988
	BD	Rau, "Dynamic Scheduling Techniques for VLIW Processors", Technical Report HPL-93-52, Hewlett-Packard Laboratories, June 1993
	BE	Rau et al., "Efficient Code Generation for Horizontal Architectures: Compiler Techniques and Architectural Support", Proceedings of the Ninth Annual International Symposium on Computer Architecture, pp. 131-139, 1982
	BF	Rau et al., "Instruction-Level Parallel Processing: History, Overview and Perspective", J. Supercomputing, Vol. 7, pp. 9-50 (1993)
	BG	Rau, et al. (Editors), "Instruction-Level Parallelism", reprint from J. Supercomputing, 7(1/2), 1993
	BH	Schuette et al., "Instruction-Level Experimental Evaluation of the Multiflow TRACE 14/300 VLIW Computer", J. Supercomputing, Vol. 7, pp. 249-271 (1993)
	BI	Silberman et al, "An Architectural Framework for Supporting Heterogeneous Instruction-Set Architectures", IEEE Computer, 26(6), pp. 39-56, June 1993
	BJ	Sites (Editor), "Alpha Architecture Reference Manual", Digital Press 1992
	BK	Smith et al., "Boosting Beyond Static Scheduling in a Superscalar Processor", IEEE Computer, pp. 344-353, 1990
	BL	Steven et al., "An Evaluation of the iHARP Multiple-Instruction-Issue Processor", Division of Computer Science, Univ. of Hertfordshire, Hatfield, Hertfordshire, pp. 1-8, 9/1995
	BM	Stone et al., "Computer Architecture in the 1990s", IEEE Computer, pp. 30-37, September 1991.
	BN	Tjaden et al., "Detection and Parallel Execution of Parallel Instructions", IEEE Transactions on Computers, C-19(10):889-895 October 1970
	BO	Uht, "Extraction of Massive Instruction Level Parallelism", Computer Architecture News, 21(3):5-12, 6/1993
	BP	The SPARC Architecture Manual, Version 8, Prentice Hall, New Jersey, 1992
	BQ	Wall, "Limits of Instruction Level Parallelism", Proceedings of the Fourth International Conference on Architectural Support for Programming Languages and Operation Systems, pp. 176-188, April 1991
	BR	Warter et al., "Enhanced Modulo Scheduling for Loops With Conditional Branches", MICRO 25, Proceedings of the 25th Annual International Symposium on Microarchitecture, pp. 170-179 (1992)
	BS	Warter et al., "The Benefit of Predicated Execution for Software Pipelining", HICSS-26 Conference Proceedings, Vol. 1, pp. 497-506, January 1993
✓	BT	Weaver et al. (Editors), "The SPARC Architecture Manual - Version 9", SPARC International Inc., PTR Prentice Hall, Englewood Cliffs, New Jersey, 1994

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